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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER | |
|---|---|
| TON, MY TRANG | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/815,800 | DATE ET AL. | |
| | Examiner | Art Unit | |
| | My-Trang N. Ton | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6,9,10,12 and 25-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12 and 39-41* is/are allowed.

6)☒ Claim(s) *1-4,9,10,25-30 and 33-38* is/are rejected.

7)☒ Claim(s) *5,6,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on 4/19/06 has been received and considered. This reference (Ref. No. JP 11-205147) appear to be the best reference with respect to the claimed invention. However, at least one limitation is not disclosed (for example: gate electrodes of a plurality of current source MISFETs ....connected to the gate electrodes of the first and second current input MISFETs" (claims 1, 25, 33, 36, 39); "the gate electrode of the second current input MISFET being electrically connected to the gate electrode of the first current input MISFET" (claims 9-10, 12).

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 4, 9-10, 25-30, 33-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Date (US 2005/0073513).

The applied reference has a one common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Date discloses in fig. 4 a display driver including:

a first current distribution MISFET (19a) of a first conductivity type, a source of the first current distribution MISFET being supplied with a supply voltage;

a first current input MISFET (10a) of a second conductivity type, a drain of the first current input MISFET (10a) being electrically connected to a drain of the first current distribution MISFET (19a), the drain and a gate electrode of the first current input MISFET (10a) being electrically connected to each other;

a second current input MISFET (12a) of the second conductivity type, a gate electrode of the second current input MISFET (12a) being electrically connected to the gate electrode of the first current input MISFET (10a), a drain and the gate electrode of the second current input MISFET (12a) being electrically connected to each other;

a plurality of current supply sections each including a current source MISFET (CM1a – CMna) of the second conductivity type, gate electrodes of the plurality of current source MISFETS (CM1a – CMna) of the plurality of current supply sections

being electrically connected to the gate electrodes of the first and second current input MISFETS (10a, 12a);

a second current distribution MISFET (21a) of the first conductivity type, a gate electrode of the second current distribution MISFET (21a) being electrically connected to a gate electrode of he first current distribution MISFET (19a), a drain of the second current distribution MISFET (21a) being electrically connected to the drain of the second current input MISFET (12a);

a third current distribution MISFET (23a) of the first conductivity type provided adjacent to the second current distribution MISFET (19a), a gate electrode of the third current distribution MISFET (23a) being electrically connected to the gate electrodes of the first current distribution MISFET (19a) and the second current distribution MISFET (21a); and

a first current output terminal (26a) being electrically connected to a drain of the third current distribution MISFET (23a) as recited in claim 1.

Regarding claim 2: a distance between the second current distribution MISFET (21a) and the third current distribution MISFET (23a) is equal to or shorter than 200 um.

Regarding claim 3: the voltage applied to gate electrode of 21a and 23a reads on a bias power supplying terminal.

Regarding claim 4: element 18a reads on an additional current distribution MISFET of the first conductivity type.

Regarding claim 9:

a first current input terminal (input applied to 12a);

a first current MISFET of a first conductivity type (12a);

a plurality of current supply sections each including a current source MISFET of the first conductivity type (CM1a – CMna);

a second current input MISFET of the first conductivity type (10a);

a bias power input terminal ( terminal applied to 21a, 23a);

a first current distribution MISFET of a second conductivity type (19a);

a second current distribution MISFET of the second conductivity type (23a);

a first current output terminal (26a);

a first current output terminal (applied to gate of 23a).

Claim 10 is similarly rejected as above:

first current input terminal (applied to 10a);

a first current input MISFET of a first conductivity type (10a);

a plurality of current supply sections each including a current source MISFET of the first conductivity type (CM1a – CMna);

a second current input MISFET of the first conductivity type (12a); and

a second current input terminal (applied to 12a).

Claim 25 is similarly rejected as claim 1:

a first current distribution MISFET (19a) of a first conductivity type;

a first current input MISFET (10a) of a second conductivity type;

a second current input MISFET (12a) of the second conductivity type;

a plurality of current supply sections each including a current source MISFET (CM1a – CMna) of the second conductivity type;

a second current distribution MISFET (21a) of the first conductivity type;

a third current distribution MISFET (23a) of the first conductivity type; and

a first current output terminal (26a).

Regarding claim 26: the plurality of current source MISFETS of the plurality of current supply sections (CM1a – CMna) are formed in a region between the first current input MISFET (10a) and second current input MISFET (12a).

Regarding claim 27: the plurality of current source MISFETS of the plurality of current supply sections (CM1a – CMna) are formed in a region extending between the first current input MISFET (10a) and second current input MISFET (12a).

Claim 28 is similarly rejected as claim 2.

Claim 29 is similarly rejected as claim 3.

Claim 30 is similarly rejected as claim 4.

Claim 33 is also similarly rejected as above claims:

a fist current input terminal (terminal applied to 10a);

a first current input MISFET of a first conductivity type(10a);

a second current input MISFET of the first conductivity type (12a);

a plurality of current supply sections including a current source MISFET of the first conductivity type (CM1a – CMna);

a bias power input terminal (terminal applied to gates 21a, 23a);

a first current distribution MISFET of a second conductivity type (21a);

a second current distribution MISFET of the second conductivity type (23a);

a first current output terminal (26a); and

a first bias power output terminal (the terminal applied to the gates of 21a, 23a).

Claims 34-35 are similarly rejected as claims 26-27.

Claim 36 is similarly rejected as claim 10.

Claims 37-38 are similarly rejected as claims 26-27 and 34-35.

***Allowable Subject Matter***

Claims 5-6, 31-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 12 and 39-41 are allowable over the prior art of record. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "a current output MISFET" in combination with "first – second current input MISFETs", "a plurality of current supply sections" and "first – third current distribution MISFETs" as recited in claims 12 and 39.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

May 15, 2006